A 60GHz-BAND LOW NOISE HJFET AMPLIFIER MODULE FOR WIRELESS LAN APPLICATIONS

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Abstract

A 60GHz-band low noise amplifier(LNA) module has been developed based on 0.15μm AlGaAs/InGaAs heterojunction FET(HJFET) technologies. A two-stage MMIC amplifier was designed and fabricated, which exhibited a noise figure less than 3dB with a gain higher than 10dB over 59.5 to 61.5GHz range. For the module fabrication, two MMIC chips were mounted in a WR-15 waveguide housing. The four-stage amplifier module demonstrated a noise figure of 4dB and a gain higher than 24dB from 59 to 60GHz. To our knowledge, this is the best reported noise figure including a microstrip-to-waveguide transition loss, using GaAs-based MMICs operating at this frequency range. The measured output power for the module at 1dB gain compression point was 4dBm. Temperature test from -20 to 70°C revealed very small noise figure and gain variations of 0.35dB and 0.62dB, respectively.

I Introduction

Increasing demand for millimeter-wave wireless communications systems has stimulated realization of low-cost small-size low-noise RX modules. In Japan, 59-60GHz band has been allocated for experimental systems by the Ministry of Post and Telecommunications. To date, several applications such as wireless LANs, cordless cameras and automotive radars[1] have been proposed at 59-60GHz band. Needless to say, an MMIC LNA is a key element in RX modules.

Recently reported GaAs-based MMICs operating at 60GHz-band include a two-stage LNA with a noise figure of 3.5dB at 58GHz[2] and a four-stage LNA with a noise figure less than 3.3dB from 58 to 62GHz[3]. An LNA module having a waveguide interface is also important for assembling millimeter-wave systems. However, there have been few reports on GaAs-based MMIC amplifier modules with waveguide interfaces, one of which is an LNA module with a noise figure of 5dB at around 60GHz[4].

This paper describes design approach and performance of a 60GHz-band two-stage monolithic LNA, which exhibited a noise figure less than 3.0dB with a gain higher than 10dB from 59.5 to 61.5GHz. A four-stage amplifier module comprising two MMICs demonstrated a noise figure of 4dB with a high gain of 24dB from 59 to 60GHz at a waveguide interface. Moreover, ambient temperature dependence of the module noise behavior has been investigated, which will be presented here.

II Circuit Design

Gate width optimization of an FET is important to obtain the best noise performance because of its parasitic effect. Especially for millimeter-wave amplifier design, parasitic capacitances of the FET should be carefully evaluated[5][6]. Based on a quantitative analysis of a scalable noise model, we have pointed out that there exists an optimum gate width (or unit finger length) considering the parasitic gate-to-drain capacitance and gate resistance[7].

An equivalent noise model for the HJFET employed in this work is shown in Fig. 1. Pospieszalski noise model[8] is used with Tg=300K and Td=2500K for a drain bias voltage(Vd) and current(Id) of 2V and 75mA/mm. The gate resistance(Rg) is proportional to the gate width, and thus, noise induced by the gate resistance reduces when the gate width is decreased, assuming the number of fingers is unchanged. The parasitic gate-to-drain capacitance(Cpf), which degrades gain, was treated as a constant value with respect to the gate width. In our 0.15μm HJFET with two gate fingers, Rg is 17Ω/mm and Cpf is 2.3fF. Parasitic source inductance also acts as a feedback element like Cpf, but was

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found to be negligible in the analysis. Intrinsic circuit parameters, and source and drain resistances are scalable with respect to the gate width.

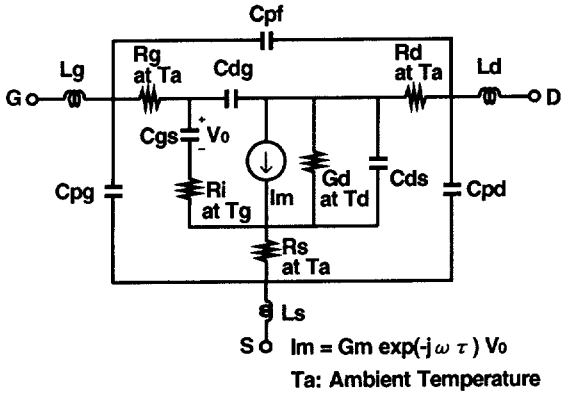

Fig. 1. Equivalent noise model for the HJFET.

Calculated minimum noise figure and associated gain at 60GHz with respect to the gate width are plotted in Fig. 2. When the gate width is increased, the minimum noise figure and gain slightly degrade due to the gate resistance increment. When the gate width is decreased to less than 30μm, the associated gain decreases rapidly due to constant Cpf. In view of achieving a high gain and a low noise figure, a gate width of 50μm has been selected for the circuit.

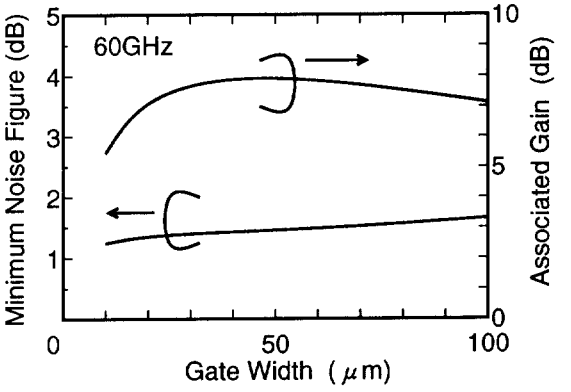

Fig. 2. Calculated gate width dependence of minimum noise figure and associated gain for the HJFET.

A circuit topology for the two-stage amplifier is represented in Fig. 3. To ensure stable operation, an interstage matching circuit with a direct impedance transformation between two stages was incorporated. RC bias networks were also designed to improve low frequency (< 30GHz) stability. The optimization criterion for the overall two-stage amplifier was a stability factor K>1 for in-band and a sufficiently high value of K>10 for out-of-band frequencies.

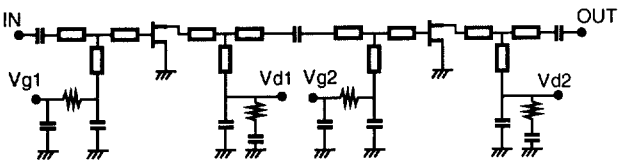

Fig. 3. Circuit topology for the two-stage MMIC LNA.

III MMIC Process and Device Characteristics

The epitaxial layer structure for an HJFET consists of an AlGaAs buffer, a 13nm undoped $In_{0.2}Ga_{0.8}As$ channel, a 33nm $Al_{0.2}Ga_{0.8}As$ layer with $5\times10^{12}cm^{-2}$ Si-planar doping and an 80nm 3 $\times10^{18}cm^{-3}$ n^+-GaAs cap layer.

In FET fabrication, mesa-isolation, conventional photolithography, electron beam evaporation and lift-off techniques have been employed. Details have been reported elsewhere[9][10]. A Metal-Insulator-Metal(MIM) structure with SiN film as a dielectric layer was applied for fabricating both dc blocking and bypass capacitors. N^+ bulk resisters were used in the bias networks.

The HJFET has a T-shaped gate cross section with 0.15μm length. The device exhibited a typical transconductance of 510mS/mm and an f_T of 96GHz at Vd=2V with a reverse gate-drain breakdown voltage of 10V. The measured minimum noise figure for the device was 0.4dB at 12GHz with an associated gain of 13dB.

IV MMIC and Module Performance

A chip photograph for the fabricated two-stage MMIC LNA is shown in Fig. 4. The chip size is 2.22mm×1.07mm. The thickness for the chip is 40μm. The noise figure and gain measured by on-wafer RF probes are plotted in Fig. 5. The LNA exhibited a noise figure less than 3.0dB with a gain higher than 10dB from 59.5 to 61.5GHz at a designed bias of Vd1=Vd2=2V and Id1=Id2=3.8mA. At 60GHz, a noise figure of 2.8dB with a gain of 12.7dB was obtained.

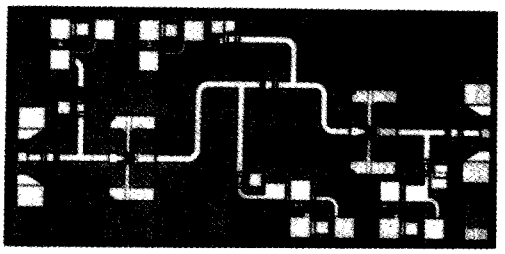

Fig. 4. Chip photograph for the fabricated two-stage MMIC LNA.

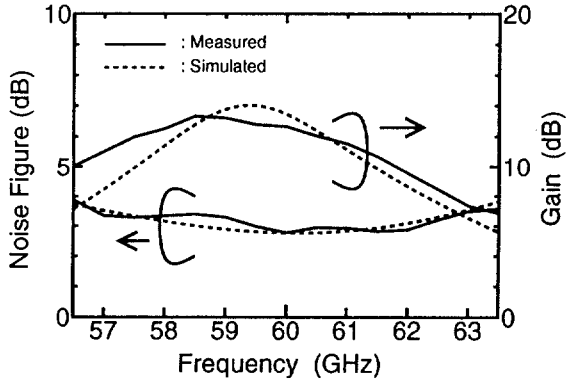

Fig. 5. Measured and simulated noise figure and gain of the two-stage MMIC LNA.

For the module, two identical MMIC chips, two 150μm-thick alumina substrates for microstrip-to-waveguide transition and bypass capacitors were mounted in a WR-15 waveguide housing. They were connected with wire bonding directly as shown in Fig. 6. No adjustment was made both on the MMIC chips and substrates. The insertion loss of this housing with end-to-end through connection was about 1.7dB.

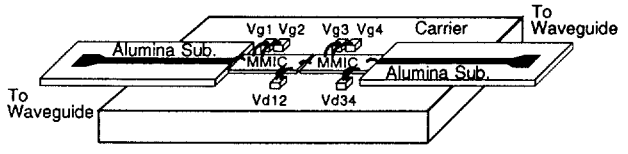

Fig. 6. Schematic view for MMIC chips and alumina substrates on a metal carrier.

The measured noise figure and gain of the fabricated four-stage amplifier module are shown in Fig. 7. The amplifier module demonstrated 4dB noise figure with over 20dB gain from 59 to 60GHz at a designed bias condition(Vd1,2=Vd3,4=2V and Id=3.8mA/stage). The input and output return losses were better than -7dB and -10dB, respectively. When the 3rd and 4th stage drain currents were increased to 7.5mA, the gain increased to over 24dB at the same frequency range while the noise figure was kept to be 4dB. Total dc power consumption was 45mW.

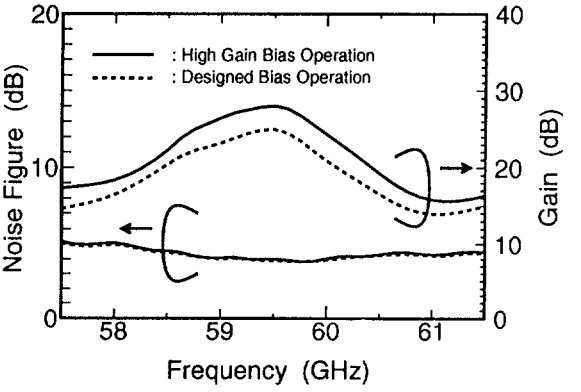

Fig. 7. Measured noise figure and gain of the four-stage LNA module. Solid lines represent data at a bias for high gain operation. Dashed lines represent data at a design bias condition.

The measured output power at 1dB gain compression point for the developed module was 4dBm at 59.5GHz. Noise figure and gain shifts as a function of the ambient temperature are depicted in Fig. 8. From -20 to 70°C, the noise figure and gain variations were reasonable values of 0.35dB and 0.62dB, respectively. In addition, no oscillation was observed at all bias and temperature conditions.

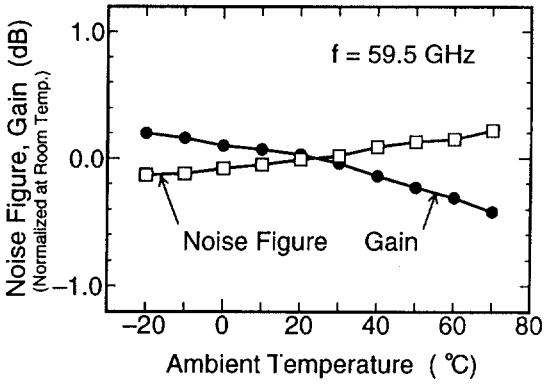

Fig. 8. Measured noise figure and gain versus ambient temperature of the module.

V Conclusions

Design approach and performance for a 60GHz-band low noise amplifier based on 0.15μm AlGaAs/InGaAs heterojunction FET technologies were described. The two-stage MMIC LNA exhibited a noise figure less than 3dB with a gain higher than 10dB over 59.5 to 61.5GHz range. The four-stage amplifier module having a waveguide interface demonstrated a noise figure of 4dB and a gain higher than 24dB from 59 to 60GHz. To our knowledge, this noise figure including a microstrip-to-waveguide transition loss is a new state-of-the-art value among GaAs-based MMICs at this frequency range. The output power at 1dB gain compression point was 4dBm. Temperature test from -20 to 70°C revealed that noise figure and gain variations were small, i.e., 0.35dB and 0.62dB, respectively. These results show great promise of the developed LNA module for 60GHz-band communications systems such as wireless LANs.

Acknowledgements

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